LinearDimensions SEMICONDUCTOR

PHYSIOsensiics™ with nanoPower Technology

IP Block: LNDADC18
<10uA Low OSR 18 Bit ΔΣ ADC
14 bit Pipeline / 6 bit Flash

GENERAL DESCRIPTION

The LNDADC18 is the lowest power consumption 18 bit (>16 bit ENOB) ADC available on the market for low bandwidth portable applications. The LNDADC18 may be programmed from an OSR (over sample rate) of 4x to 32x. At 4x and 2.5kHz clocking frequency, a 312.5Hz signal may be reliably acquired using only 7.23uA in the ADC. Alternatively, a higher clocking rate such as 32x will allow acquisition of signals up to 2.5kHz with 16 bits of accuracy or lower bandwidth signals to greater than 16 bits ENOB.

To achieve this FOM (power consumption per acquisition) the LNDADC18 utilizes the latest cascade architecture, high order delay line quantizer, and switched capacitor and subthreshold techniques.

Achieving a low OSR, high bit accuracy ADC is difficult as the low OSR requires a higher order noise transfer function (NTF) which creates instability and reduces dynamic range and/or a higher order quantizer which generally requires a complex digitally tuned flash ADC. To optimize stability and dynamic range the LNDADC18 uses a cascade architecture with a 5 bit quantizer and a 2nd order modulator.

The 5 bit quantizer utilizes the latest tracking delay line techniques to reduce the tuning and silicon overhead of conventional ADCs. The cascade allows the equivalent of a higher order NTF by cascading data converters but as the cascade is not in the timing critical loop it can utilize a twelve (12) bit self correcting pipeline architecture. The flow diagram of this arrangement is shown in Figure 2.

Each of the three ADCs may be used independently and the clock rate increased to acquire higher bandwidth signals or improve resolution in the case of the ΔΣ. The ΔΣ includes all required anti-aliasing & decimation filters and a low power subsystem (nanoPOWER) manager.

FFT – 2.5kHz. 4x OSR. 7.23uA

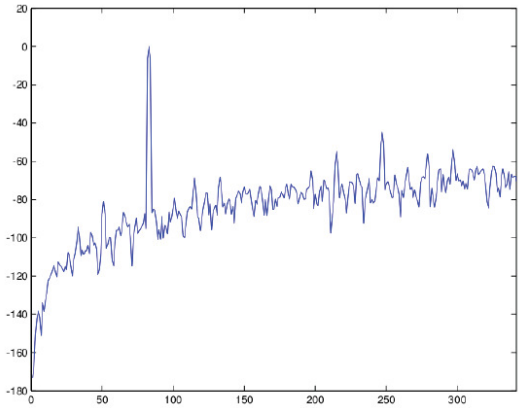

Figure 1 – FFT shows a >96 SQNR sinewave for a low LNDADC18 OSR of 4x. This represents the lowest possible current consumption for portable applications such as medical acquisition. The OSR of the ΔΣ may be adjusted to improve SQNR (ENOB) or raise the bandwidth of acquisition.

FEATURES

- Lowest current 18 bit ADC for low bandwidth (<=2.5kHz) applications
- Uses the latest switchcap and subthreshold techniques to minimize current draw
- Low OSR cascade design optimizes stability & minimizes current consumption
- Minimum clock of 2.5kHz minimizes current consumption but allows 16 bit ENOB
- Programmable OSR (oversample rate) allows tradeoff of ENOB (equivalent number of bits) to resolution
- >96dB SQNR (>16 ENOB)
- 5 bit differential delay line quantizer
- Three analog to digital converters (ADCs) form the cascade:
  - 6 bit delay line flash ADC (<1uA typ)
  - Up to 14 bit pipeline ADC (<4uA typ)
  - Up to 18 bit low OSR ΔΣ ADC (<8uA typ – ΔΣ includes the 6 bit and 14 bit ADCs)
- Flash and pipeline may be used independently
- Includes corner correcting decimation filters
- Includes antialiasing filters
- Includes 32 bit shuffling DAC structure for coefficients
- Each ADC may be put to sleep to save power
- Power optimization subsystem
- SPI Interface (independently enabled)

DIAGRAM

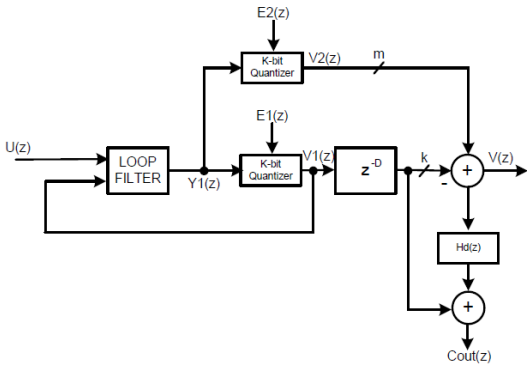

Figure 2 – Cascade arrangement of the 18 bit **ΔΣ** ADC

APPLICATIONS

- Portable heart rate equipment
- Portable fitness & wellness products
- Non-critical diagnostics
- Low bandwidth portable electronics
- Vibration sensors

14 Bit ADC

The LNDADC14 block is a very low current (typical 3.5uA in 14 bit mode and 2.7uA in 10 bit mode) analog to digital converter developed for low bandwidth battery operated portable electronics applications. The LNDADC14 block uses the latest techniques in low current data converter design. These newly derived techniques obsolete many of the existing low current implementations with respect to their power per conversion figure of merit (FOM). The LNDADC14 block may be used independently or represents the second stage cascade of the 18 Bit ΔΣ ADC block.

The LNDADC14 block operates from 2.7 to 3.6V Vin and operates at a minimum 2.5kHz clock rate. The LNDADC14 block features a user settable resolution from 8 to 14 bits to optimize power savings (for example a signal may be sampled at 8 bits until it meets certain criteria and then resolution improved to 14 bits to improve feature accuracy at the price of more current for a period of time).

The LNDADC14 block utilizes a 1.5 bit self correcting quantizer and fully differential internal analysis engine making it extremely tolerant to noise, battery glitches, and comparator metastability. An example of this self correcting capability is shown in Figure 3 (this is an 8 bit example).

For extremely low current applications of limited bandwidth (<1uA) the LNDADC14 block may be utilized in a wakeup and sleep mode due to its fast startup time (<100us). The LNDADC14 utilizes <100nA of current in sleep mode.

The LNDADC14 block features an ENOB of >12 bits in 14 bit mode and >9 bits in 10 bit mode, an INL of +/-0.65 LSB and DNL of +/-0.45 LSB.

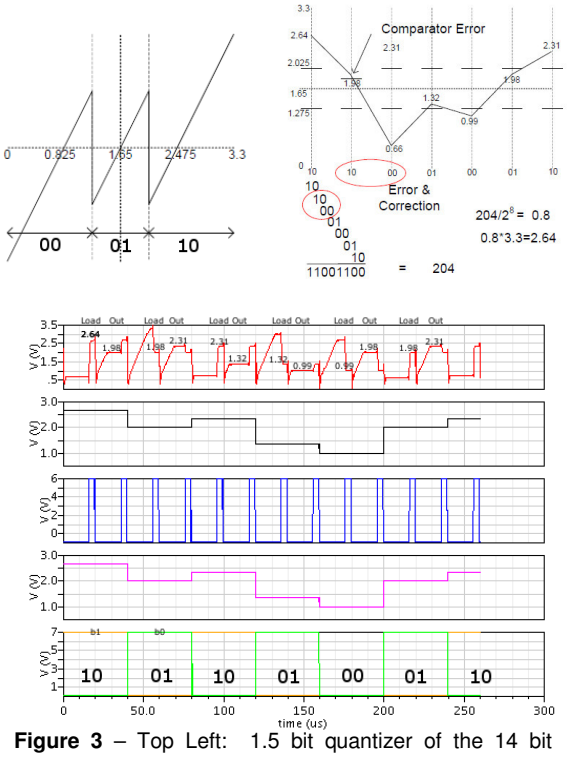

Figure 3 – Top Left: 1.5 bit quantizer of the 14 bit pipeline ADC; Top Right: Self correcting operation of the quantizer and; Bottom: Waveforms of the 14 bit ADC.

6 Bit Flash ADC

The 5 bit quantizer of the ΔΣ is created from a 6 bit flash converter. The flash converter utilizes a differential delay line technique (see Figure 4) to reduce tuning and silicon requirements. An accurate transconductor and reference delay line allow accurate conversions of >5 bit ENOB.

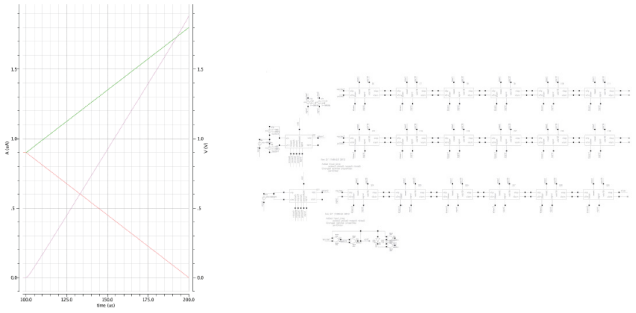

Figure 4 – Left: Optimized transconductor for use with differential delay line; Right: Partial differential delay line with reference delay line.

DECIMATION AND ANTIALIASING

The LNDADC18 includes antialiasing filtering and decimation filtering with correction to ensure accurate conversion within the signal band of interest. Figure 5 shows part of this filter in the form of a sinc response. Additional digital filters and correction filters are required to optimize the response. Figure 5 also shows the shuffling DACs used to feedback the digitized information within the ΔΣ loop and reduce tuning overhead.

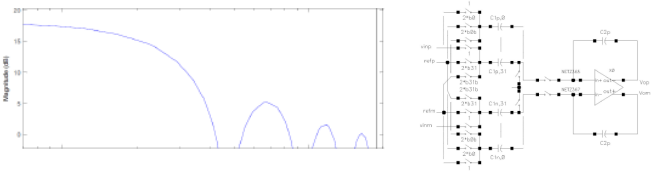

Figure 5 – Left: Partial decimation filter sinc response; Right: 32 element shuffling DAC.